ABSTRACT

0030 A semiconductor process wafer having substantially co-planar active areas and a laser marked area in an adjacent inactive area and method for forming the same to eliminate a step height and improve a subsequent patterning process over the active areas wherein an inactive area trench is formed overlying the laser marked area in parallel with formation of STI trenches in the active area whereby the active areas and the inactive area are formed substantially co-planar without a step height.